UBA2072

Low Voltage Full-bridge control IC for CCFL backlighting

Rev. 08.0 — February 2007 **Preliminary data sheet**

DRAFT DRAFT DRAFT DRAFT DRAFT

1. General description

The UBA2072 is a low voltage IC intended to drive Cold Cathode Fluorescent Lamps (CCFLs) for back-lighting applications. The IC contains level-shifters, bootstrap diodes and drivers for the external full-bridge power switches.

Furthermore, the UBA2072 has a build-in HF oscillator which determines the operating frequency, a phase shift controller for obtaining constant lamp current, and a PWM generator which is used to set the brightness level of the CCFLs.

The UBA2072 is designed to operate over a wide low voltage inverter supply range, up to 30V. The IC can be supplied directly from the inverter supply.

2. Features

- Wide supply voltage range (9 V to 30 V DC)
- Adjustable maximum fault timing
- Integrated level-shifters
- Integrated bootstrap diodes
- Lamp current control
- Over-voltage control
- Over-current protection
- Ignition failure detection
- Arcing detection
- Brightness level adjustment through PWM dimming
- Integrated PWM generator

3. Applications

LCD-backlighting, including LCD-TV and LCD-Monitor applications. The IC is intended to drive and control a full-bridge inverter with resonant load circuit for CCFLs, but can also drive an array of External Electrode Fluorescent Lamps (EEFLs).

founded by Philips

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
UBA2072T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UBA2072TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

5. Block diagram

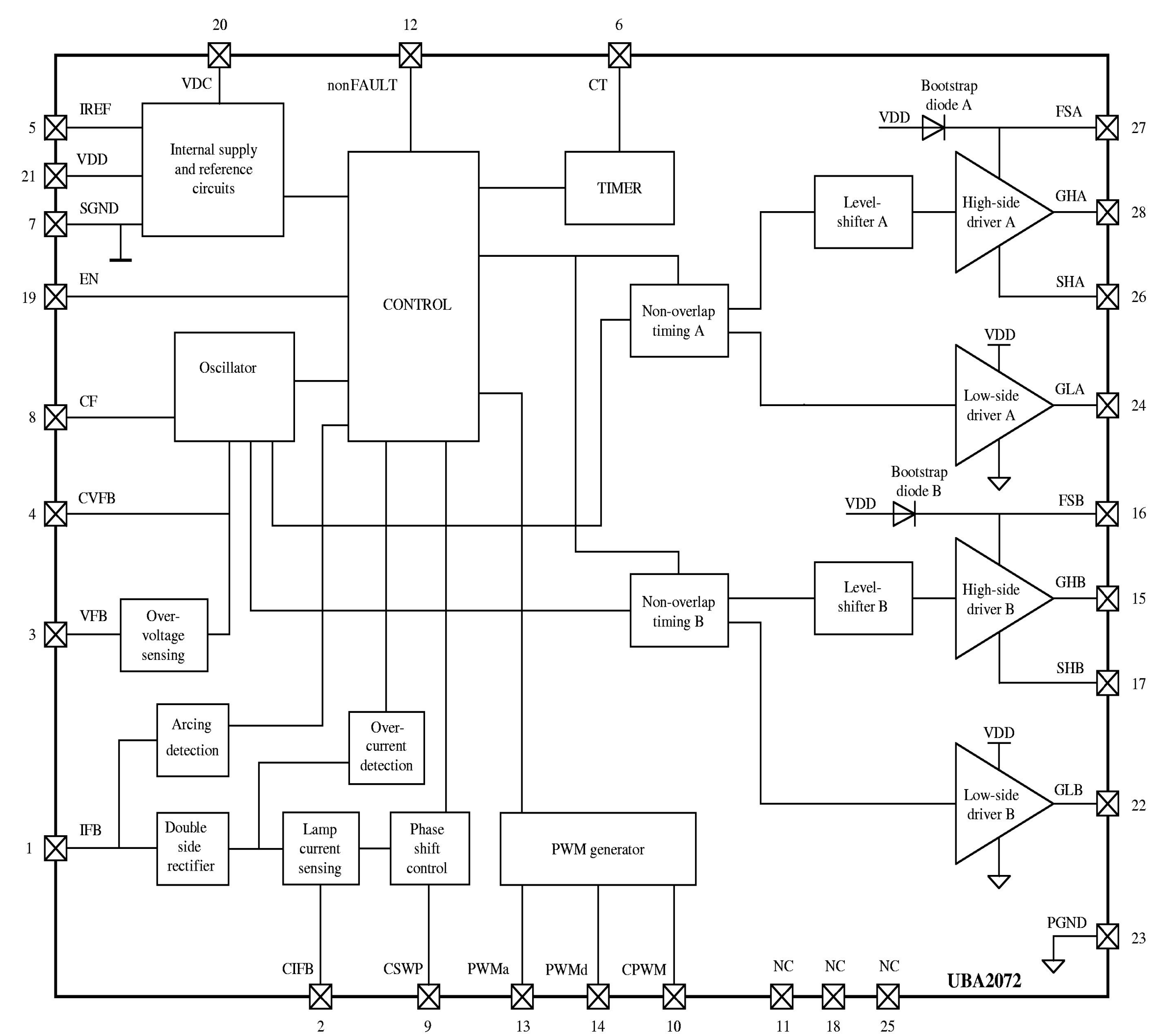


Fig 1. Block diagram UBA2072.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

6. Pinning information

6.1 Pinning

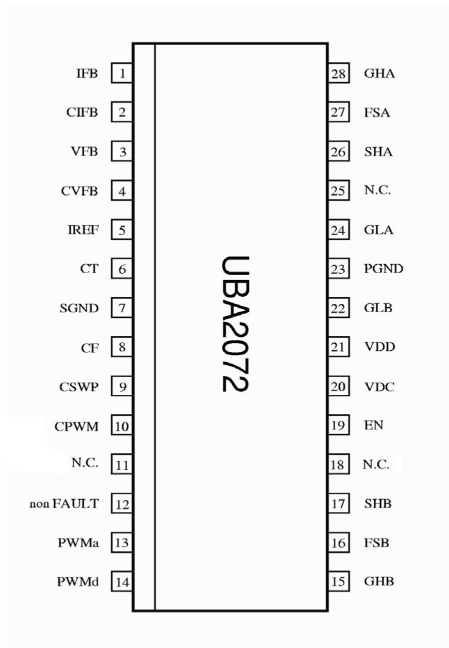


Fig 2. Pin assignment SO28 and SSOP28 package (top view)

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description	Function
IFB	1	current feedback input.	Input signal for the lamp current control loop. Should be connected to a voltage proportional to the lamp current.
CIFB	2	current regulation capacitor.	A capacitor must be connected between this pin and the signal ground. It sets the time constant of the lamp current control loop.
VFB	3	voltage feedback input	Input signal for the voltage control loop. Should be connected to a voltage proportional to the transformer output voltage
CVFB	4	voltage regulation capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time constant of the voltage control loop.
IREF	5	reference current output	A 33kΩ resistor must be connected between this pin and the signal ground. The IC uses it to make accurate internal currents.
CT	6	fault timing capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time that a fault condition is allowed before the IC shuts itself down.
SGND	7	signal ground	
CF	8	HF-oscillator timing capacitor	A capacitor must be connected between this pin and the signal ground. It sets the minimum switching frequency of the full bridge.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

Table 2: Pin description *...continued*

Symbol	Pin	Description	Function
CSWP	9	phase-shift sweep capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time in which the phase difference between bridge halve A and bridge halve B is swept down from regulation level to zero or swept up from zero to regulation level during PWM dimming.
CPWM	10	PWM timing capacitor	If a capacitor is connected between this pin and the signal ground, it sets the frequency of the PWM oscillator. If this pin is connected to signal ground the internal PWM oscillator is disabled.
NC	11	not connected	
nonFAULT	12	status signal input/output	The IC signals a fault condition to an external circuit by pulling this pin low and external circuits can also signal a fault condition to the IC by pulling this pin low.
PWMa	13	analog PWM dimming input	The dutycycle of the internally generated PWM signal is proportional to the voltage on this pin.
PMWd	14	digital PWM dimming input/output	Digital output of internally generated PWM signal if a capacitor is connected to the CPWM-pin. Digital input of PWM signal if the CPWM-pin is connected to signal ground. *Note that the signal on the PWMd-pin is active low, so low voltage on the PWMd-pin means lamps are on.*
GHB	15	high-side driver output B	Gate connection of the high side power switch of full bridge halve B
FSB	16	floating supply output B	A buffer capacitor must be connected between this pin and the SHB-pin. This capacitor is charged when the low side switch B is on and supplies the high side driver B.
SHB	17	high-side source connection B	Return for high side gate driver B. Must be connected to the source of the high side power switch of full bridge halve B.
NC	18	not connected	
EN	19	chip enable input	A low voltage on this pin will reset and shutt down the IC
VDC	20	IC low-voltage supply input	IC supply
VDD	21	regulated 12 V supply output/input	A buffer capacitor must be connected between this pin and power ground
GLB	22	low-side driver output B	Gate connection of the low side power switch of full bridge halve B
PGND	23	power ground	return for low side drivers A and B
GLA	24	low-side driver output A	Gate connection of the low side power switch of full bridge halve A
NC	25	not connected	
SHA	26	high-side source connection A	Return for high side gate driver A. Must be connected to the source of the high side power switch of full bridge halve A.
FSA	27	floating supply output A	A buffer capacitor must be connected between this pin and the SHA-pin. This capacitor is charged when the low side switch A is on and supplies the high side driver A.
GHA	28	high-side driver output A	Gate connection of the high side power switch of full bridge halve A

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

7. Functional description

The UBA2072 is designed to drive a full-bridge inverter with resonant load. The load consists typically of transformers with CCFLs. Two parameters are used by the UBA2072 to control the switches of the full-bridge inverter: the phase shift and the switching frequency.

The two full bridge halves A and B (Figure 3) always operate at the same switching frequency. The frequency is used to control transformer output voltage during the first ignition of the lamps. The phase difference between the full-bridge halves A and B voltages (V_A and V_B) controls the lamp current, as this determines the rms value of the full-bridge inverter voltage V_A - V_B (Figure 4).

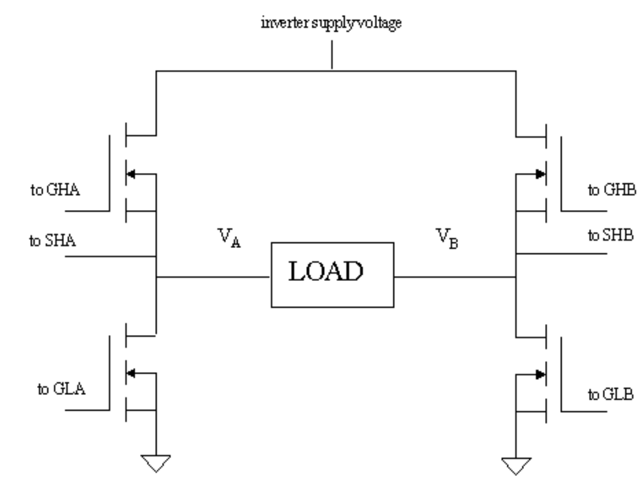


Fig 3. Full-bridge inverter definition

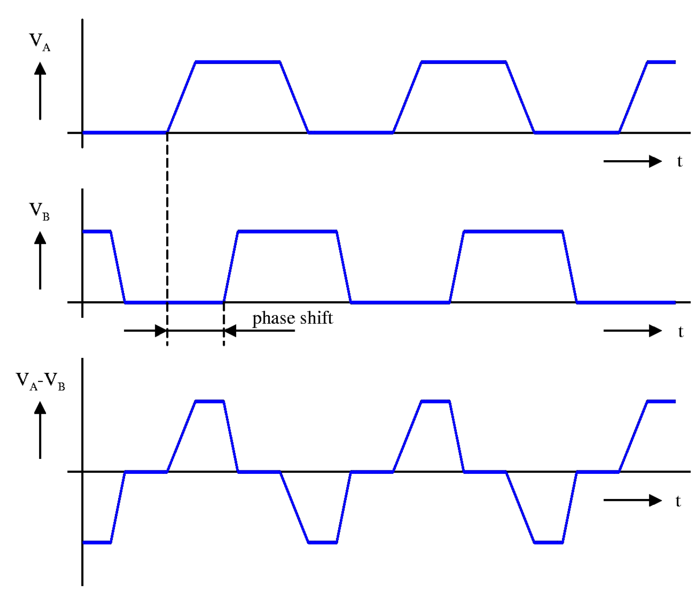


Fig 4. Full-bridge inverter voltage and definition of phase shift

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

7.1 IC Supply

The VDC pin is connected to an external supply with a voltage of 9 V to 30 V. The VDD-pin must be connected to a buffer capacitor (see Figure 5). The VDD-pin acts as a regulated 12 V output, from which the gate drivers are supplied. External auxiliary circuits may also be supplied from the VDD pin. **Never supply the IC directly via the VDD-pin.** VDC-pin voltage must always[1] be above VDD-pin voltage.

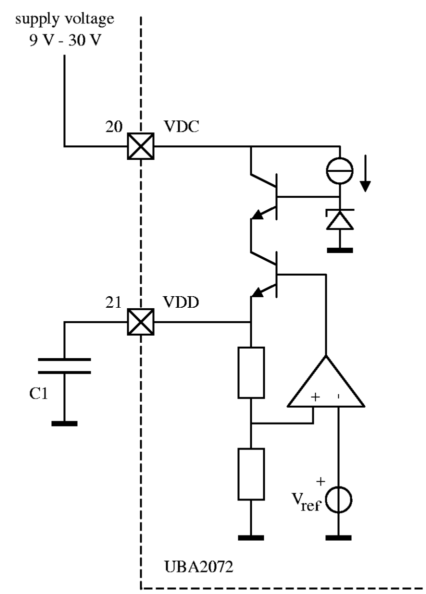


Fig 5. IC supply configuration

7.2 Start-up and Under-Voltage Lock-Out (UVLO)

The IC starts up at $V_{VDC(start)}$ and locks out (stops oscillating) when the voltage on the VDC-pin drops below $V_{DC(stop)}$.

7.3 Enable

The UBA2072 is put in standby when the voltage on the EN-pin comes below $V_{EN(low)}$ (see Table 5). The IC will stop oscillating, and most of the internal circuits will shut down. However, the internal linear regulator between VDC and VDD will remain active, but with reduced current supply capability. All internal signals are reset when the EN-pin is low.

When the voltage on the EN-pin comes above $V_{EN(high)}$ the IC will start up again.

7.4 Lamp (re-)ignition

The IC starts at its maximum switching frequency $F_{s(max)}$. First the capacitors at the CIFB-pin and CSWP-pin are charged (setting the phase shift between the two bridge halves to maximum). Then the frequency is swept down to the minimum frequency $F_{s(min)}$ (see Figure 7). During this initial ignition frequency sweep the lamp voltage will increase

1. During normal operation. During switch off faster fall down of VDC with respect to VDD is acceptable.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

as the frequency comes closer to the resonant frequency of the unloaded resonance circuit. Once the ignition voltage V_{ign} is reached, the lamps will ignite and the lamp voltage will drop to the voltage of the loaded resonance curve.

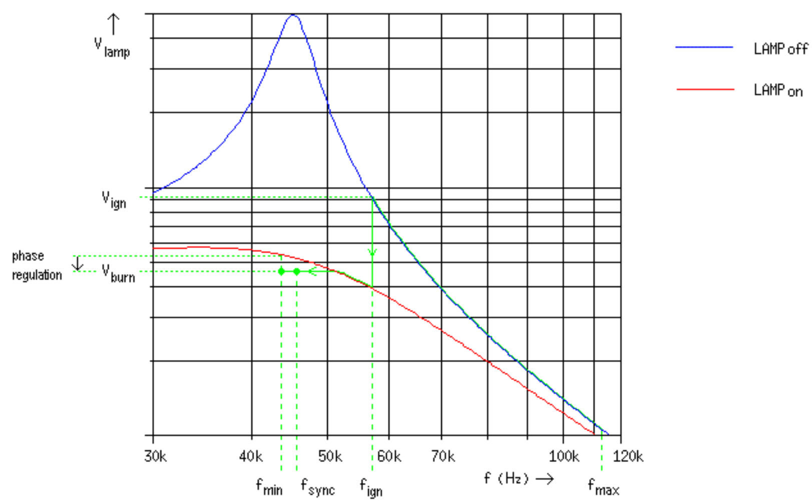


Fig 6. Initial ignition of flourescent lamp via frequency sweep and load resonance .

Advantage of the sweep rather then a fixed ignition frequency is that sensitivity for spread in resonance frequency is much lower.

Once the lamps are ignited the frequency sweep down continues, gradually increasing the lamp current (the resonance circuit should now still be inductive, so current increases as frequency drops) untill the current regulation level is reached and the current regulation loop starts decreasing the phase shift between the bridge halves in order to keep the lamp current constant. If the current regulation loop cannot decrease the phase shift fast enough to counteract the frequency sweep down, then the frequency sweep is slowed down. Once the frequency has reached Fs(min), PWM dimming is enabled (See Figure 7).

Initial ignition frequency sweep and PWM-generator are not synchronised, and once the frequency sweep is finished PWM dimming can start anywhere in its cycle.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

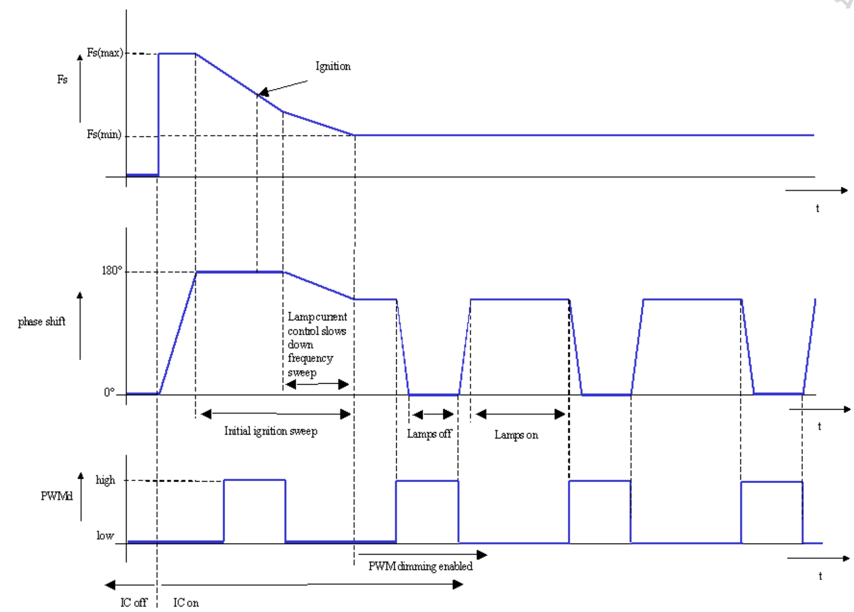


Fig 7. Timing diagram of the initial ignition frequency sweep

During PWM dimming the switching frequency is constant. Only the phase shift is swept from its regulated value to its minimum value and back. The phase shift sweep has to provide re-ignition of the lamps, therefor the unloaded resonance curve of Figure 6 has to be high enough at the normal operation switching frequency Fs(min).

The voltage at the CVFB-pin is inverse proportional to the switching frequency,(see Figure 8). The voltage at the CVFB-pin is clamped at the voltage $V_{CVFB(range)}$ were the switching frequency is Fs(min).

The voltage at the CSWP-pin is proportional to the phase shift (see Figure 8). The voltage at the CSWP-pin is clamped at the low side at $V_{CSWP(lclamp)}$ and at the high side at V_{CIFB}. Because V_{CIFB} is clamped at $V_{CIFB(hclamp)}$, V_{CSWP} is also clamped.

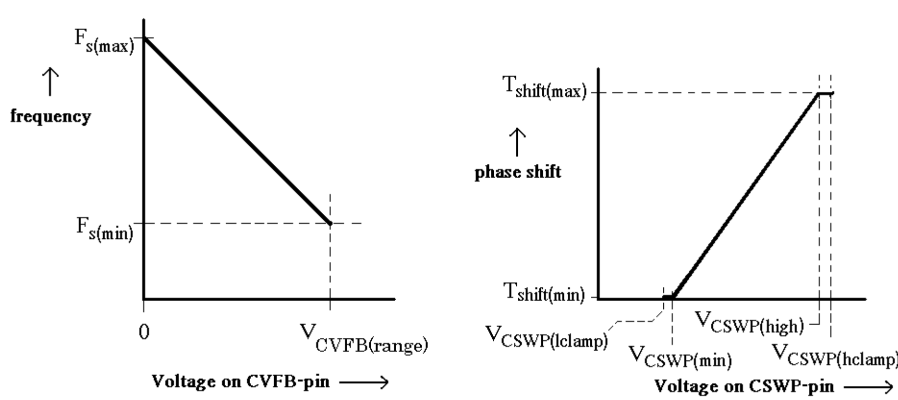


Fig 8. frequency and phase shift as function of CVFB and CSWP voltages

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

7.5 Lamp current control

The lamp current control is active during the initial ignition frequency sweep and when the lamps are on. It is disabled during the time within a PWM dim cycle that the lamps are off.

An (AC or DC) voltage representing the lamp current, usually the voltage across an external sense resistor, is to be connected to the IFB-pin. This voltage is internally double-side rectified (DSR), and compared to a reference level $V_{IFB(reg)}$ by an operational transconductance amplifier (OTA), as shown in Figure 9.

When the current is being regulated, switches S1 and S2 (see Figure 9) are closed (conducting). The output current of the OTA is fed into capacitor C1, which is connected to the CIFB-pin. The voltage across this capacitor is copied into capacitor C2, which is connected to the CSWP-pin. The voltage on the CSWP-pin controls the phase shift.

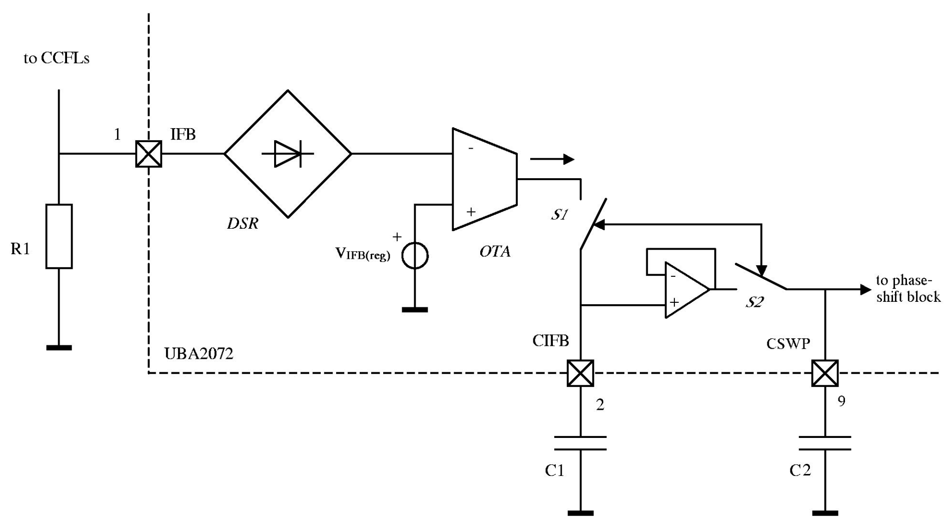


Fig 9. Lamp current control circuit

7.6 PWM dimming

During the time within a PWM dim cycle that the lamps are off, switches S1 and S2 are opened (non-conducting). In this way the regulation level is stored in C1 when the current regulation loop is opened (see Figure 9).

After the regulation loop is opened, C2 is discharged (the voltage on the CSWP-pin is swept down) to switch off the lamps, and charged again to turn the lamps on again. The lamps on versus off time is determined by the signal on the PWMd-pin (low = lamps on).

The minimum phase difference between the bridge halves during the lamps off period of each PWM cycle is $\Delta\phi_{(min)}$.

During the PWM lamps off period the phase shift level at which the lamp current was in regulation is preserved in the capacitor connected to the CIFB-pin (C1 in Figure 9). Switches S1 and S2 are closed (conducting) again when the voltage on the CSWP-pin has reached the voltage on the CIFB-pin again.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

The phase shift sweep speed is determined by the capacitor connected to the CSWP-pin (C2 in Figure 9). The real lamp light output will be slightly less then the PWMd signal duty cycle because of the phase shift sweep time (see Figure 10). When the lamp-on time is too short to sweep up the voltage on the CSWP-pin, the IC will wait until the CSWP voltage has actually reached the current control level before sweeping down again. This prevents that the lamps go out completely when deep dimming is combined with a too large capacitor at the CSWP-pin.

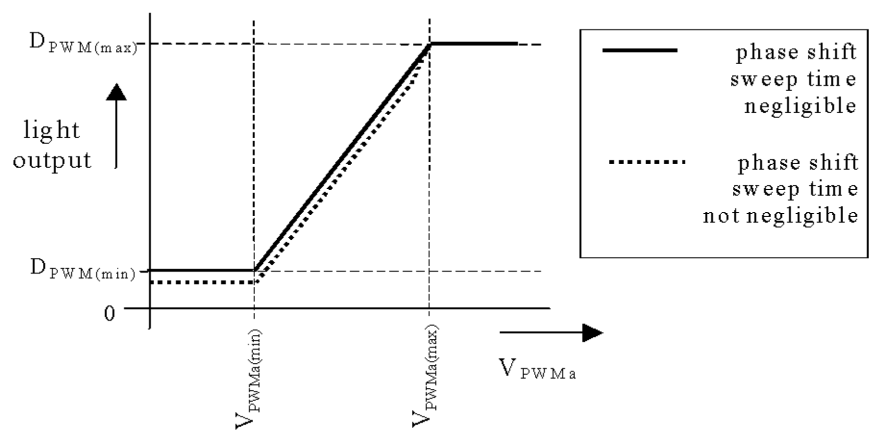


Fig 10. Light output as function of PWMa input voltage

Three pins are available to configure the internal PWM generator: the CPWM-, PWMa-, and the PWMD-pin. The two possible PWM configurations are shown in Figure 11. In the analog or master mode the internal PWM generator is active and generating the PWM signal. This signal is put on the PWMd-pin, which is automatically configured as an output. The minimum dutycycle of the internal PWM generator is limited to $D_{PWM(min,intern)}$.

When the CPWM-pin is connected to ground, the IC is put in digital or slave mode. The PWMd-pin is then an input and the IC uses the PWM signal provided on the PWMd-pin.

The signal on the PWMd-pin is active low. A voltage below $V_{PWMD(low)}$ on the pin will turn the lamps on and a voltage above $V_{PWMD(high)}$ will turn the lamps off.

PWM dimming of multiple ICs can be synchronised by configuring one IC as master and the others as slaves and connecting all PWMd-pins together.

PWM dimming is only enabled in normal mode, when no fault condition excists. The only exception is when an external detected fault condition is entered via the nonFAULT-pin, then PWM dimming remains active (see Figure 13).

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT

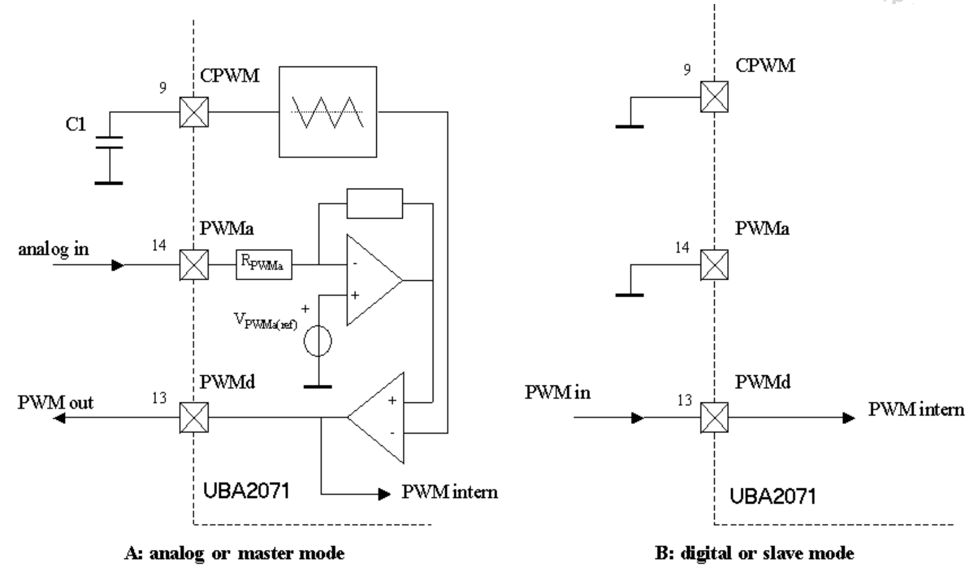


Fig 11. PWM dimming configurations

7.7 The fault timer

The fault timer provides a delay inbetween the detection of a fault and the shut down of the IC (enter STOP-state). Its time $T_{fault(timeout)}$ is proportional to the capacitor connected to the CT-pin.

Any fault condition will start the timer. When the timer is activated, the capacitor at the CT-pin will be alternatingly charged and discharged (see Figure 12). These cycles are being counted by a four bit counter. After one cycle (the fault signalling delay $T_{fault(delay)}$) the nonFAULT-pin is activated (pulled low), to signal to any external circuit that there is a fault detected and the IC will stop if that fault continues. After 15 cycles is the fault time-out period $T_{fault(timeout)}$ reached, and the IC will enter STOP-state.

If the fault timer is inactive, the CT-pin voltage is one Vbe (≅0.7V). The CT-timer has a protection that prevents the IC to start-up if the CT-pin is shorted to GND.

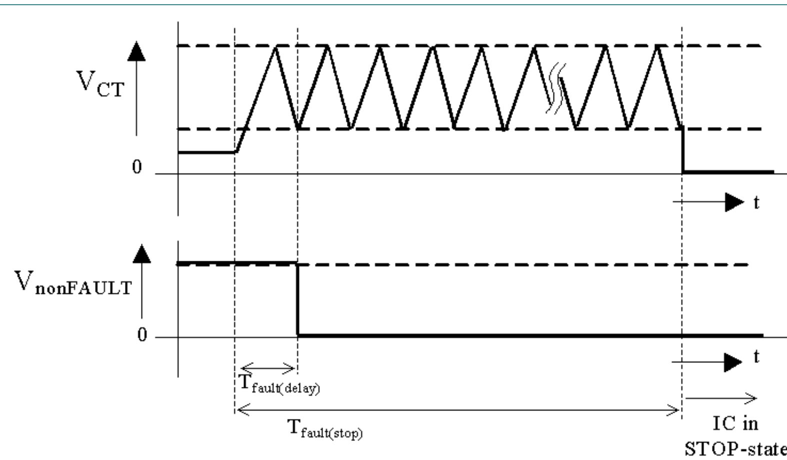


Fig 12. Fault timer wavefporms

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

7.8 Protections

All fault conditions and how they are processed in the IC can be found in Figure 13.

The UBA2072 includes internal over voltage (OV), overcurrent (OC), bad contact or arcing (ARC) and ignition failure (IF) protections. There is also one pin (the nonFAULT-pin) which provides bidirectional fault signalling to and from any external circuit. Via this pin a lamp short detection or over temperature detection or such can be added.

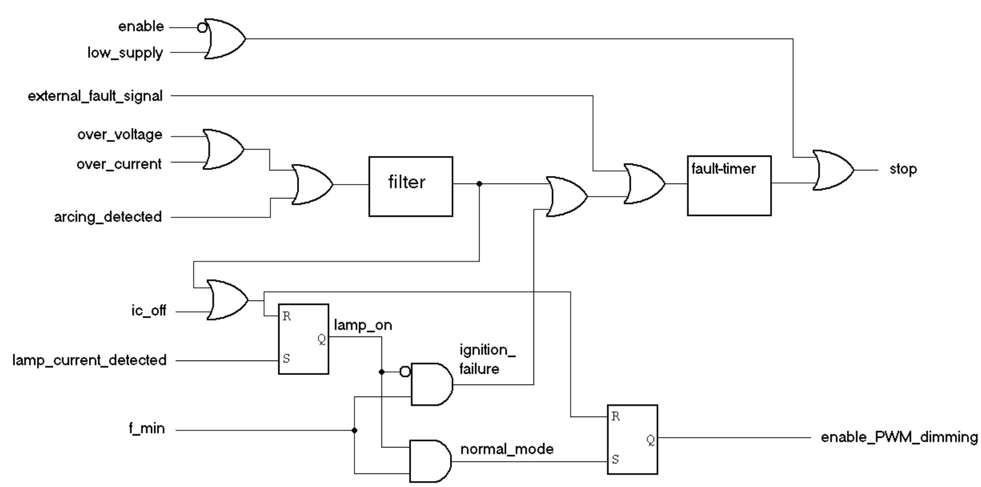


Fig 13. Simplified control schematic.

In the next sections each fault protection function will be explained.

7.8.1 Over voltage protection

The over voltage protection circuit is intended to prevent the transformer output voltage from exceeding its maximum rating. It can also be used to regulate the output voltage to the required lamp ignition voltage.

When the voltage on the VFB-pin exceeds the OV reference level $V_{VFB(ovref)}$, over voltage is detected. As result PWM dimming is disabled and the fault timer is started. Also the capacitor connected to the CVFB-pin is discharged (by $I_{CVFB(ov)}$). When the voltage at the VFB-pin drops below the OV reference level, the CVFB capacitor is charged (by $I_{CVFB(charge)}$) again.and the output voltage of the transformer will increase again. Because the charging and discharging of the CVFB capacitor follows the ripple on the VFB voltage, the feedback gain of the voltage control loop is set by the ripple on the feedback signal.

If CVFB is more discharged then charged (over a hf cycle) then the CVFB voltage will drop, and the switching frequency increase. As a result the output voltage of the transformer will decrease[2]. When this happens the current control loop is froozen (switch S1 of Figure 9 is opened (non-conducting), so the regulation level stored in C1 cannot be changed by the current regulation loop) in order to prevent the frequency increase being compensated by a phase shift difference increase by the current control.

2. Presuming that the effective full bridge load impedance is in inductive region.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

An internal latch makes the OV fault signal continuesly high even if the voltage at the VFB-pin only exceeds VVFB(ovref) during part of the output period. So the peak of the voltage on the VFB-pin determines if an over voltage fault condition is seen.In order to avoid that OV fault condition at the nominal switching frequency (with the lamps operating normally), the voltage ripple on the VFB-pin must not be too large.

The voltage at CVFB is limited by the oscillator circuit to $V_{CVFB(range)}$ when the minimum switching frequency $F_{s(min)}$ is reached. This ensures an immediate frequency increase capability at over voltage detection.

7.8.2 Over current detection

When the absolute value[3] of the voltage across the current sense resistor (connected to the IFB-pin) exceeds the OC reference level $V_{IFB(ocref)}$, over-current is detected. As result PWM dimming is disabled and the fault timer is started.

7.8.3 Arcing detection

If arcing occurs, for instance due to a bad lamp connection, it causes repetitive short current spikes that can be seen as voltage spikes at the IFB input[4]. The arcing detection circuit is directly connected to the IFB-pin, so it can only see spikes with a positive polarity. Usually that will be sufficient. It can detect spikes with amplitude above $V_{IFB(arcref)}$ and a duration longer then $T_{SPIKE(min)}$. Each spike will trigger an internal one-shot, which signals to the control circuits that arcing has been detected. If this happens PWM dimming is disabled, and the fault timer is started.

7.8.4 Ignition Failure (IF)

When the current control loop comes close to its regulation point, the lamps are presumed to be on (ignited). This is when the average double side rectified IFB-pin voltage is above $V_{IFB(lampon)}$. If the lamps are not on when the ignition sweep is finished (switching frequency has reached $F_{S(min)}$), then an ignition failure is detected, PWM dimming is disabled and the fault timer is started.

7.8.5 The nonFAULT-pin

The nonFAULT-pin provides bidirectional signalling of the fault status between the IC and any external circuit. When no fault is detected, the voltage on the pin is pulled high by an internal current source.

An external circuit can signal to the IC that a fault has been detected by pulling down the pin. The IC will detect the current drawn from the pin and start the fault timer. To prevent interference with the PWM dimming, the IC will only look at the nonFAULT pin during the period that the lamp current regulation loop is closed (VCSWP=VCIFB).

When the IC detects a fault internal (as in Section 7.8.1 to Section 7.8.4), it signals this via the nonFAULT pin by pulling the pin down. In this case the IC can not see anymore if there's an external detected fault, but that's no problem, because the faulttimer is then already running.

3. The OC comparator is behind the double side rectifier at the IFB-pin
4. Provided that the current sensing circuit is simple sense resistor only.

© NXP B.V. 2007. All rights reserved.

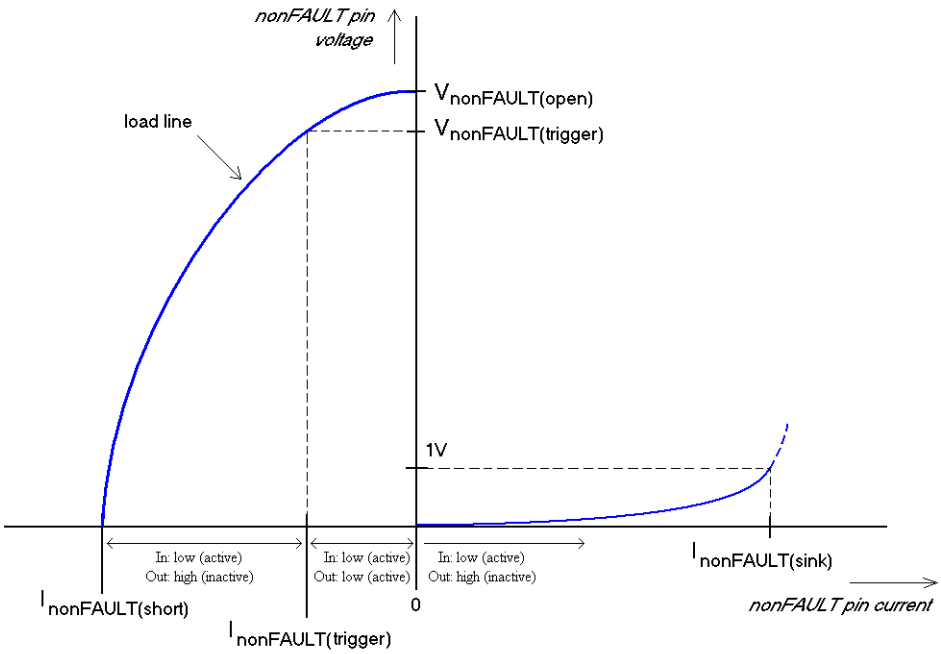


Fig 14. Input and output levels at the nonFAULT pin.

The signal from the IC is a voltage signal and the signal to the IC is a current signal. In this way a driving conflict is prevented. Also it leaves the possibility for the outside world to see the signal from the IC even while a fault condition is being signalled to the IC in the mean time, as illustrated in Figure 15.

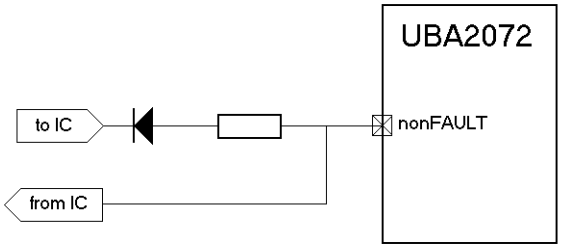


Fig 15. Splitting the nonFAULT pin signals to and from the IC.

7.9 High- and low-side drivers

The four drivers are identical. The output of each driver is connected to the equivalent gate of an external power MOSFET. The bootstrap capacitors are charged from the VDD voltage when the low-side power MOSFETs are turned on, and they supply the high-side drivers. The VDD voltage directly supplies the low-side drivers. Current sourcing capability and the on-resistance of the drivers can be found in Table 5.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

7.10 Non overlap

For each half bridge a delay is made between the switching-off of the external high side power transistor and the switching-on of the external low side power transistor and the other way round. The duration is the so called 'non-overlap' time (T_{NONOV}).

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 7); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
General					
R_{IREF}	reference resistor value on pin IREF		30	36	kΩ
SR	slew rate on pins FSA, FSB, GHA, GHB, SHA, and SHB		–4	+4	V/ns
T_{amb}	ambient temperature		–25	+100	°C
T_j	junction temperature		–25	+125	°C
T_{stg}	storage temperature		–55	+150	°C
Voltages					
V_{SHA}, V_{SHB}	voltage on pins SHA and SHB		0	+30	V
V_{FSA}, V_{FSB}	voltage on pins FSA and FSB	with respect to V_{SHA}, V_{SHB}	-0.3	+14	V
V_{EN}	voltage on pin EN		-0.3	+14	V
V_{GLA}, V_{GLB}	voltage on pins GLA and GLB		-0.3	V_{VDD}	V
V_{GHA}	voltage on pins GHA		V_{SHA} -0.3	V_{FSA}	V
V_{GHB}	voltage on pins GHB		V_{SHB} -0.3	V_{FSB}	V
V_{PGND}	voltage on pin PGND		0	0	V
V_{VDC}	voltage on pin VDC		-0.3	+30	V
V_{PWMa}, V_{PWMd}, $V_{nonFAULT}$	voltage on pins PWMa, PWMd and nonFAULT		-0.1	+5	V
V_{VFB}	voltage on pin VFB	continuous	-0.1	+5	V
		t<1ms	-0.1	+8	V
V_{IFB}	voltage on pin IFB	continuous	-5	+5	V
		t<100µs	-9	+9	V
ESD					

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

Table 3: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 7); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage				
	human body model	IFB, CIFB, VFB, CVFB, IREF, CT, CF, CSWP, CPWM, nonFAULT, PWMa, PWMd, EN, VDC, VDD, GLA, GLB	-2	+2	kV
		GHB, FSB, SHB, SHA, FSA, GHA	-1	+1	kV
	machine model	all pins	-250	+250	V
Latchup					
	SNW-FQ-303	all pins			

9. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; SO28 package	68	K/W
		in free air; SSOP28 package	108	K/W

10. Characteristics

Table 5: Characteristics

T_{amb} = 25 °C; V_{VDC} = 15 V; V_{EN}=V_{VDD}; C_{VDD}=100nF; R_{IREF} = 33 kΩ and CPWM pin connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (pin 7); currents are positive when flowing into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Start-up							
$V_{VDC(start)}$	start-up voltage level			8.6	9	9.4	V
$V_{VDC(stop)}$	stop voltage level			7.7	8	8.3	V
$V_{VDC(hys)}$	start-stop hysteresis level			0.9	1	1.1	V
Supply							
$I_{VDC(on)}$	total supply current on pin VDC	oscillating	[1]			5	mA
$I_{VDC(on)}$	total supply current on pin VDC	VDC=30V; oscillating	[1]			7.5	mA
$I_{VDC(off)}$	total supply current on pin VDC	V_{EN}=0V				1.5	mA
$I_{VDC(off)}$	total supply current on pin VDC	VDC=30V; V_{EN}=0V				2	mA
$V_{VDD(reg)}$	Regulated voltage on pin VDD	VDC=30V; V_{EN}=0V		11.3	12	12.7	V
$V_{VDD(reg)}$	Regulated voltage on pin VDD at maximum supply current	non-oscillating; I_{VDD}=-36mA		11			V
V_{VDC}-V_{VDD}	Dropout voltage VDD regulator	VDC=10V; oscillating;	[1]		1.5		V
V_{boot}	voltage drop bootstrap diode	I_{FSA} = I_{FSB} = 5mA			1.5		V
Ignition							
$F_{s(max)}$ / $F_{s(min)}$	VCO frequency ratio			2.2	2.4	2.6	
$V_{CVFB(range)}$	VCO voltage range				2.5		V
$I_{CVFB(charge)}$	CVFB charge current	V_{VFB}=2V, V_{CVFB}=2V		-24	-21	-18	µA

 © NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

Table 5: Characteristics *...continued*

T_{amb} = 25 °C; V_{VDC} = 15 V; V_{EN}=V_{VDD}; C_{VDD}=100nF; R_{IREF} = 33 kΩ and CPWM pin connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (pin 7); currents are positive when flowing into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Normal operation							
$F_{s(min)}$	minimum switching frequency	C_{CF} = 100 pF		43.0	44.8	46.6	kHz
$F_{s(min)}$	minimum switching frequency			10		100	kHz
$V_{IFB(reg)}$	current regulation reference level			1.24	1.32	1.40	V
$V_{IFB(min)}$	minimum voltage of lineair operating range				- 2.5		V
$V_{IFB(max)}$	maximum voltage of linear operating range				2.5		V
R_{IFB}	input impedance IFB pin	V_{IFB} = 1V			40		kΩ
R_{IFB}	input impedance IFB pin	V_{IFB} = -1V			20		kΩ
K_{IFB}	transconductance OTA			13	16	19	µA/V
Drivers							
$I_{driver(source)}$	sourcing current of drivers	V_{GLA}, V_{GLB}, V_{GHA}, V_{GHB} = 1V, V_{VDD} = V_{FSA} = V_{FSB}=12V		-180	-145	-110	mA
$R_{driver(sink)}$	sinking resistance of drivers	V_{GLA}, V_{GLB}, V_{GHA}, V_{GHB} = 1V, V_{VDD} = V_{FSA} = V_{FSB}=12V				7.3	Ω
T_{nonov}	non-overlap time			0.45	0.55	0.65	µs
PWM dimming							
F_{PWM}	PWM frequency			100		1000	Hz
F_{PWM}	PWM frequency	C_{CPWM} = 33 nF		308	324	340	Hz
$\Delta\phi_{(min)}$	minimum phase shift				0		°
$\Delta\phi_{(max)}$	maximum phase shift				180		°
$V_{CSWP(low)}$	CSWP voltage resulting in $\Delta\phi_{(min)}$				1		V
$V_{CSWP(high)}$	CSWP voltage resulting in $\Delta\phi_{(max)}$				3		V
$V_{CIFB(hclamp)}$	high CIFB clamp voltage				3.1		V
$V_{CSWP(lclamp)}$	low CSWP clamp voltage				0.95		V
$I_{CSWP(charge)}$	CSWP charge current			-24	-21	-18	µA
$I_{CSWP(discharge)}$	CSWP discharge current			18	21	24	µA
R_{PWMa}	input impedance PWMa pin				100		kΩ
$V_{PWMa(min)}$	input voltage on PWMa pin for minimum PWM duty cycle				1.24		V
$V_{PWMa(max)}$	input voltage on PWMa pin for maximum PWM duty cycle				3		V
$D_{PWM(min,intern)}$	minimum PWM duty cycle		[2]		12		%
$D_{PWM(min,extern)}$	minimum PWM duty cycle	CPWM pin connected to SGND	[2]		0		%
$D_{PWM(max)}$	maximum PWM duty cycle		[2]		100		%
$I_{PWMD(source)}$	source capability PWMd output	V_{PWMd}=3V			-1		mA
$I_{PWMD(sink)}$	sink capability PWMd output	V_{PWMd}=1V			1		mA

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

Table 5: Characteristics *...continued*

T_{amb} = 25 °C; V_{VDC} = 15 V; V_{EN}=V_{VDD}; C_{VDD}=100nF; R_{IREF} = 33 kΩ and CPWM pin connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (pin 7); currents are positive when flowing into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PWMD(high)}$	logic high input level on PWMd				1.7	V
$V_{PWMD(low)}$	logic low input level onPWMd		0.85			V
Protections						
$V_{VFB(ovref)}$	over voltage reference level		2.40	2.52	2.64	V
$I_{CVFB(ov)}$	CVFB discharge current	V_{VFB}>$V_{VFB(ovref)}$, V_{CVFB}=2V	18	21	24	µA
$V_{IFB(lampon)}$	lamp on detection level			0.9		V
$V_{IFB(ocref)}$	over current reference level		2.65	3.0	3.3	V
$V_{IFB(arcref)}$	minimum detectable arcing spike amplitude			5		V
$T_{SPIKE(min)}$	minimum detectable arcing spike duration			200		ns
$T_{fault(delay)}$	fault output delay time	C_{CT} = 100 nF	0.063	0.069	0.075	s
$T_{fault(stop)}$	fault stop time	C_{CT} = 100 nF	0.85	0.95	1.05	s
$V_{nonFAULT(open)}$	open pin voltage on nonFAULT		4.7	5.0	5.3	V
$V_{nonFAULT(trigger)}$	input trigger voltage on pin nonFAULT		3.8	4.3	4.8	V
$I_{nonFAULT(trigger)}$	input trigger current of nonFAULT pin		-32	-27	-22	µA
$I_{nonFAULT(3V)}$	low input nonFAULT pin current	$V_{nonFAULT}$ = 3V	-220	-190	-160	µA
$I_{nonFAULT(short)}$	short circuit current on pin nonFAULT	$V_{nonFAULT}$ = 0V	-240	-210	-180	µA
$I_{nonFAULT(sink)}$	maximum low output current on pin nonFAULT	$V_{nonFAULT}$ = 1V	0.75	1	1.5	mA
Chip enable levels						
$V_{EN(high)}$	logic high level on pin EN				1.7	V
$V_{EN(low)}$	logic low level on pin EN		0.9			V

[1] GLA, GLB, GHA and GHB open.

[2] PWMd is active low: A low level on the PWMd pin corresponds with lamps on. Example: D_{PWM}=20% means PMWd is during 20% of each cyle low and the lamps are 20% of the time on, resulting in een light output of 20%.

11. Application information

Figure 16 shows an example backlighting configuration, where the inverter and the IC are supplied from the same DC voltage. Two lamp are connected, each to another output of the same transformer. The leakage inductances of this transformer provides the ballast impedances for the lamp. An analogue voltage is converted to a PWM signal to provide for the desired brightness level. Optional lamp short detection is via the lamp voltage sensing and D13, D23 and the nonFAULT-pin is indicated.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

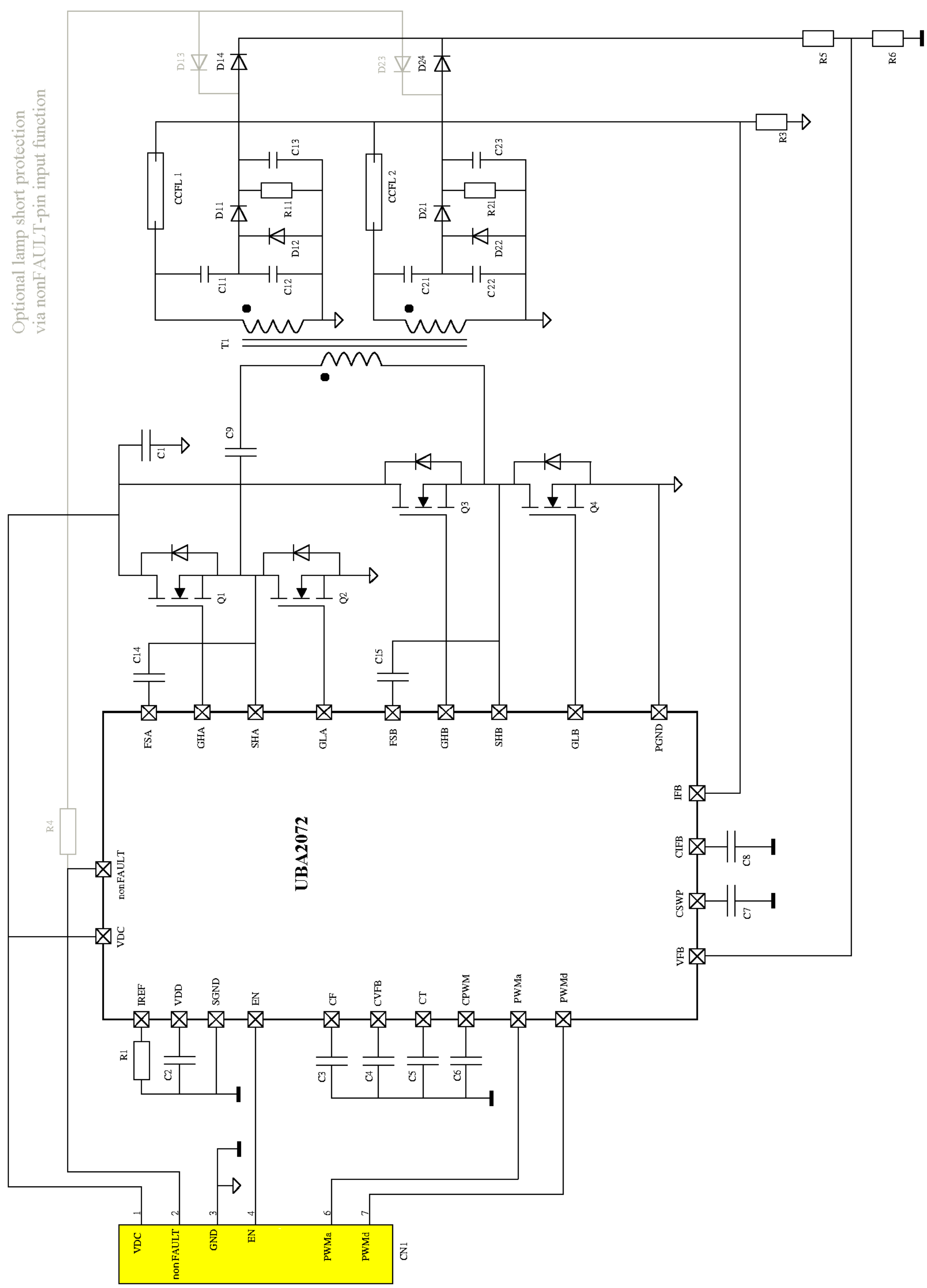


Fig 16. Example backlighting application diagram

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

12. Test information

12.1 Quality information

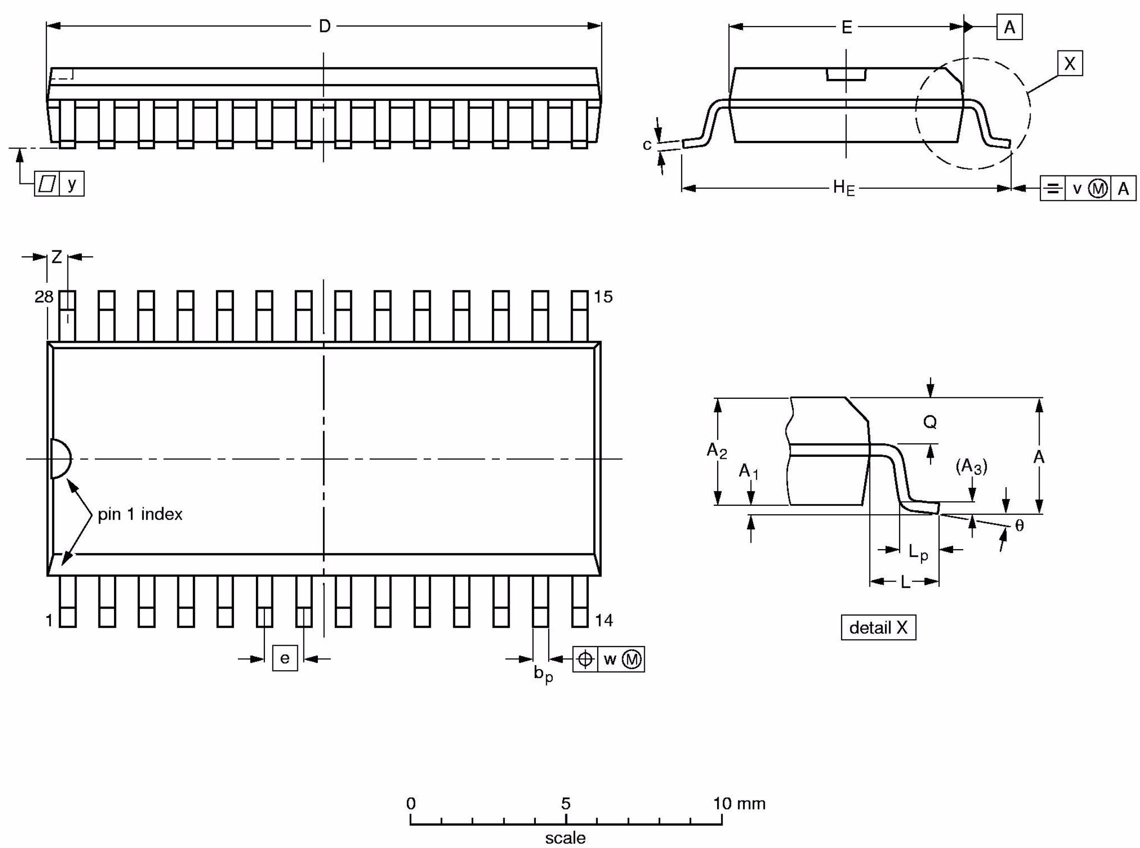
The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

13. Package outline

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

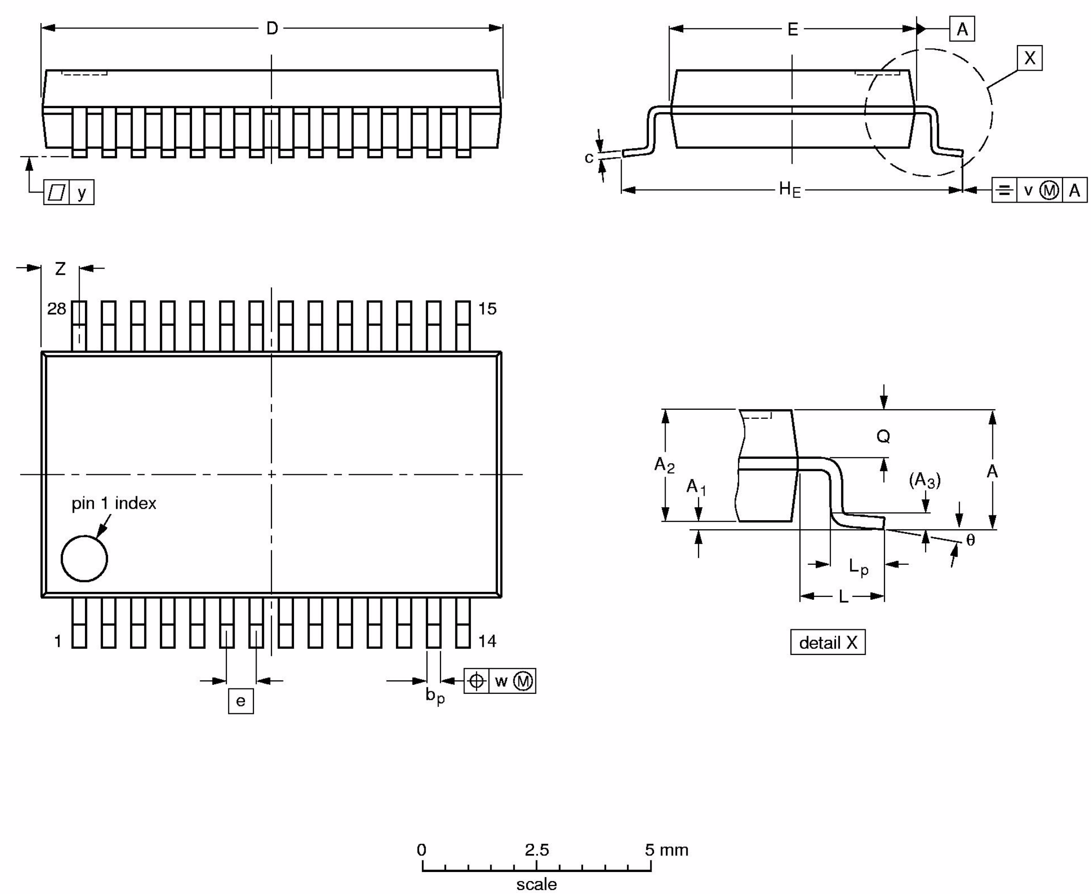
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

Fig 17. Package outline SO28 (SOT136-1)

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

Fig 18. Package outline SSOP28 (SOT341-1)

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

14. Soldering

14.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

14.2 Through-hole mount packages

14.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 Surface mount packages

14.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA and SSOP-T packages

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

14.4 Package related soldering information

Table 6. Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package[1]	Soldering method		
		Wave	Reflow[2]	Dipping
Through-hole mount	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable[3]	–	suitable
Through-hole-surface mount	PMFP[4]	not suitable	not suitable	–
Surface mount	BGA, LBGA, LFBGA, SQFP, SSOP-T[5], TFBGA, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[6]	suitable	–
	PLCC[7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[7][8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended[9]	suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] Hot bar soldering or manual soldering is suitable for PMFP packages.

[5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

15. Revision history

Table 7: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
UBA2072_1	2004 12	Objective data	-	xxxx xxx xxxxx	-
UBA2072_2	2005 04	Objective data	-	xxxx xxx xxxxx	
UBA2072_3	2005 04	Objective data	-	xxxx xxx xxxxx	
UBA2072_4	2005 10	Objective data	-	xxxx xxx xxxxx	
UBA2072_5	2006 04	Objective data	-	xxxx xxx xxxxx	
UBA2072_6	2006 06	Objective data	-	xxxx xxx xxxxx	
UBA2072_7	2006 08	Preliminary data	-	xxxx xxx xxxxx	
UBA2072_8	2007 02	Preliminary data	-	xxxx xxx xxxxx	-
			-	xxxx xxx xxxxx	
			-	xxxx xxx xxxxx	
			-	xxxx xxx xxxxx	
			-	xxxx xxx xxxxx	
			-	xxxx xxx xxxxx	
			-	xxxx xxx xxxxx	

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT

15.1 Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

15.2 Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

15.3 Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

16. Trademarks

16.1 Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **sales.addresses@www.nxp.com**

© NXP B.V. 2007. All rights reserved.

DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT

17. Contents

© NXP B.V. 2007. All rights reserved.